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EXAMINER	
PWU, JEFFREY C	

ART UNIT	PAPER NUMBER
2143	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Notice of Allowability	Application No. 09/941,702	Applicant(s) BUCH ET AL.	
	Examiner Jeffrey C. Pwu	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/22/2006 Interview*.

2. ☒ The allowed claim(s) is/are *1-38*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *6/23/06* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Paul Steiner Reg. No. 41,326 on 6/23/2006.

The application has been amended as follows:

IN THE CLAIMS:

Claims have been amended as follows:

1. (currently amended) A method of optimizing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing N network interface cards (NICs), a first one of the N NICs being dedicated to receiving an incoming data stream;

binding an interrupt from the first one of the N NICs to a first one of the N processors;

binding an interrupt for an nth NIC to an nth processor, wherein $0 < n <= N$; and

binding a deferred procedure call (DPC) for the nth NIC to the nth processor, wherein $0 <= n <= N$.

2. (original) The method of claim 1, further comprising tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer.

3. (previously amended) The method of claim 1, further comprising binding P server threads to specific ones of the second through Nth processors, wherein P is a positive integer.

4. (previously amended) The method of claim 2, further comprising binding P server threads to specific ones of the second through Nth processors, wherein P is a positive integer.

5. (previously amended) The method of claim 1, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

6. (previously amended) The method of claim 2, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

7. (previously amended) The method of claim 3, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

8. (previously amended) The method of claim 4, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

9. (currently amended) A method of providing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing N network interface cards (NICs); ~~and~~

dedicating a first one of said N NICs to receiving an incoming data stream;

tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer and wherein $0 < n <= N$; and

binding an interrupt from the first one of said N NICs to a first one of said N processors.

10. (previously amended) The method of claim 9, further comprising binding P server threads to specific ones of the second through Nth processors, wherein P is a positive integer.

11. (previously amended) The method of claim 10, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

12. (previously amended) The method of claim 9, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

13. (currently amended) A method of providing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing N network interface cards (NICs); ~~and~~

dedicating a first one of said N NICs to receiving an incoming data stream;

binding an interrupt from the first one of said N NICs to a first one of said N processors; and

binding P server threads to specific ones of the second through Nth processors.

14. (previously amended) The method of claim 13, further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

15. (previously amended) A method of providing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

16. (previously amended) The method of claim 5, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

17. (previously amended) The method of claim 6, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

18. (previously amended) The method of claim 7, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

19. (previously amended) The method of claim 8, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

20. (previously amended) The method of claim 11, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

21. (previously amended) The method of claim 14, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

22. (previously amended) The method of claim 15, further comprising improving first level cache efficiency by increasing a time quantum allotted to server threads which process streaming data buffers.

23. (previously amended) A multiprocessor data server comprising:

N processors, wherein N is an integer greater than or equal to 2;

N network interface cards (NICs), a first one of said N NICs being dedicated to receiving an incoming data stream;

wherein an interrupt from the first one of said N NICs is bound to a first one of said N processors; and

wherein an interrupt for an nth NIC is bound to an nth processor, $0 < n <= N$; and

wherein a deferred procedure call (DPC) for said nth NIC is bound to said nth processor.

24. (original) The multiprocessor data server of claim 23, further comprising M client connections, wherein said M client connections are tightly coupled to said nth processor via said nth NIC, M being a positive integer.

25. (previously amended) The multiprocessor data server of claim 23, further comprising P server threads, wherein said P server threads are bound to specific ones of the second through Nth processors.

26. (previously amended) The multiprocessor data server of claim 24, further comprising P server threads, wherein said P server threads are bound to specific ones of the second through Nth processors.

27. (previously amended) The multiprocessor data server of claim 23, further comprising first and second level caches for each of said N processors, wherein instructions and temporal data are stored in said second level caches of said N processors, and wherein non-temporal data is stored in first level caches of said N processors, bypassing the second level caches.

28. (previously amended) The multiprocessor data server of claim 24, further comprising first and second level caches for each of said N processors, wherein instructions and temporal data are stored in said second level caches of said N processors, and wherein non-temporal data is stored in first level caches caches of said N processors, bypassing the second level caches.

29. (previously amended) The multiprocessor data server of claim 25, further comprising first and second level caches for each of said N processors, wherein instructions and temporal data are stored in said second level caches of said N processors, and wherein non-temporal data is stored in first level caches caches of said N processors, bypassing the second level caches.

30. (previously amended) The multiprocessor data server of claim 26, further comprising first and second level caches for each of said N processors, wherein instructions and temporal data are stored in said second level caches of said N processors, and wherein non-temporal data is stored in first level caches caches of said N processors, bypassing the ~~L2~~ second level caches.

31. (currently amended) A program storage device, readable by a machine, embodying a program of instructions executable by the machine to perform a method of providing scalability in a multiprocessor data server having N processors, wherein N is an integer greater than or equal to 2, the method comprising:

implementing N network interface cards (NICs), a first one of the N NICs being dedicated to receiving an incoming data stream;

binding an interrupt from the first one of the N NICs to a first one of the N processors;

binding an interrupt for an nth NIC to an nth processor, wherein 0 < n < = N; and

binding a deferred procedure call (DPC) for the nth NIC to the nth processor, wherein 0 <= n < = N.

32. (original) The program storage device of claim 31, the method further comprising tightly coupling M client connections to the nth processor via the nth NIC, wherein M is a positive integer.

33. (previously amended) The program storage device of claim 31, the method further comprising binding P server threads to specific ones of the second through Nth processors, wherein P is a positive integer.

34. (previously amended) The program storage device of claim 32, the method further comprising binding P server threads to specific ones of the second through Nth processors, wherein P is a positive integer.

35. (previously amended) The program storage device of claim 31, the method further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

36. (previously amended) The program storage device of claim 32, the method further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

37. (previously amended) The program storage device of claim 33, the method further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

38. (previously amended) The program storage device of claim 34, the method further comprising:

defining first and second level caches for each of the N processors;

storing instructions and temporal data in second level caches of the N processors; and

storing non-temporal data in first level caches of the N processors, bypassing the second level caches.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey C. Pwu whose telephone number is 571-272-6798. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 571-272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

6/26/06
JEFFREY PWU
PRIMARY EXAMINER